(digital signal having an image information). The latch (A) 603 writes in and maintains an n-bit digital signal which is supplied by the external of the source signal line driver circuit 601 in order simultaneously with the input of the above-mentioned timing signals.

Note that the digital signals may be sequentially inputted to the plurality of latch stages of the latch (A) 603 when the digital signals are taken in by the latch (A) 603. However, the present invention is not limited to this structure. A so-called division drive may be performed, that is, the plurality of latch stages of the latch (A) 603 is divided into a number of groups, and then the digital signals are parallel inputted to the respective groups at the same time. Note that the number of groups at this point is called a division number. For example, if the latch circuits are grouped into 4 stages each, then it is called a 4-branch division drive.

The time necessary to complete writing of the digital signals into all the latch stages of the latch (A) 603 is called a line period. In effect, the above-defined line period added with the horizontal retrace period may also be referred to as the line period.

After the completion of one line period, a latch signal is supplied to the latch (B) 604. In this moment, the digital signals written in and held by the latch (A) 603 are sent all at once to the latch (B) 604 to be written in and held by all the latch stages thereof.

Sequential writing-in of digital signals on the basis of the timing signals from the shift register 602 is again carried out to the latch (A) 603 after it has completed sending the digital signals to the latch (B) 604.

During this second time one line period, the digital video signals written in and held by the latch (B) 603 are inputted to the source signal lines.

Fig. 7B is a block figure which is showing a structure of the gate signal line driver circuit.

The gate signal driver circuit 605 has a shift resister 606 and a buffer 607 respectively. According to circumstances, the level shifter can be provided.

In the gate signal line driving circuit 605, the timing signal is supplied to the buffer 607 from the shift register 606, and this is supplied to a corresponding gate signal line. Gate electrodes of the switching TFTs of one line portion of pixels are connected to each of the gate signal lines. All of the switching TFTs of the one line portion of pixels must be placed in an ON state simultaneously, and therefore a buffer in which a large electric current can flow is used.

In the case that the repair method of the present invention is used, the switching TFT is in an ON state by controlling a signal inputted to the gate signal line by the gate signal line driver circuit, and the EL driver TFT is in an ON state by a digital signal inputted to the source signal line from the source signal line driver circuit.

Further, in this embodiment, the structure of the driver circuit of the pixel portion shown in Embodiment 1 is explained, but also the structure of the driver circuit of the pixel portion shown in Embodiment 2 has the same structure. The pixel portion shown in Embodiment 2 has a two gate signal line driver circuit, and each gate signal line driver circuit has structures shown in Fig. 7B respectively. In Embodiment 2, each gate signal line driver circuit control the inputting signal to the writing gate signal line and the eraser gate signal line respectively.

[Embodiment 4]

A description given in this embodiment is of a structure of a driving circuit for driving the pixel portion of the light emitting device shown in Embodiment 1. The structure of this embodiment is different from the one described in Embodiment 3. A source signal line driving circuit and a gate signal line driving circuit for driving the pixel

portion of Embodiment 1 may not necessarily have the structure shown in this embodiment.

Fig. 8A is a circuit diagram of a source signal line driving circuit 611 according to this embodiment. Reference numeral 612 denotes a shift register; 613, a level shifter; and 614, a sampling circuit.

A clock signal (CLK) and a start pulse signal (SP) are inputted to the shift register 612. An analog signal containing image information (analog video signal) is inputted to the sampling circuit 614.

Upon input of the clock signal (CLK) and the start pulse signal (SP) in the shift register 612, a timing signal is generated and inputted to the level shifter 613. The timing signal inputted to the level shifter 613 is inputted to the sampling circuit 614 with its amplitude amplified.

Using the timing signal inputted to the sampling circuit 614, the analog video signal also inputted to the sampling circuit 614 is sampled and then inputted to the associated source signal line.

Fig. 8B is a block diagram showing the structure of a gate signal line driving circuit.

A gate signal line driving circuit 615 has a shift register 616 and a buffer 617. The circuit may also have a level shifter.

In the gate signal line driving circuit 615, a timing signal is supplied from the shift register 616 to the buffer 617, and then to the associated gate signal line. The gate signal line is connected to gate electrodes of switching TFTs in one line of pixels. Since switching TFTs in one line of pixels have to be turned ON at once, the buffer used has to be capable of flowing a large current.